What is claimed is:

1. An image array having a plurality of pixels disposed in rows and columns, wherein each pixel includes a photodiode, a thin film transistor (TFT), and a clamping diode, the image array further comprising:

a plurality of data lines,

a plurality of gate lines,

a plurality of bias lines carrying a bias voltage, and

a plurality of clamp lines electrically interconnecting the clamping diodes in individual ones of the rows or columns of the array, wherein the clamp lines carry a clamping voltage.

2. The image array of claim 1, wherein the clamping diode in each pixel is electrically connected between a storage node of the photodiode and the clamp line.

3. The image array of claim 1, wherein the clamping voltage keeps the photodiode under reverse bias.

4. The image array of claim 3, wherein the clamping voltage is between about -4 to -5 V with respect to the potential of the data line.

5. The image array of claim 1, wherein the clamping diode has a forward bias when the photodiode becomes overexposed.

6. The image array of claim 5, wherein the clamping diode has a forward bias of about 0.1 V at the initial stages of overexposure.

7. The image array of claim 1, wherein the bias voltage is about -8 to -10 volts.

8. A clamping circuit in a sensor array that reduces lag comprising:

a gate line;

a data line;

a bias line carrying a bias voltage V_{bias};

a clamp line carrying a clamping voltage V_{clamp};

a TFT having a source, a drain, and a gate, wherein the source or drain of the TFT is connected to the data line and the gate is connected to the gate line;

a photodiode having an anode, a cathode, and a storage node, wherein the anode is connected to the other of the source or drain of the TFT and the cathode is connected to the bias line; and

a clamp diode having an anode and cathode, wherein the clamp diode anode is connected to the clamp line and the clamp diode cathode is connected to the storage node of the photodiode.

9. A full fill factor image array having a plurality of pixels disposed in rows and columns, wherein each pixel includes a photodiode, a first thin film transistor (TFT), and a second TFT, the image array further comprising:

a plurality of data lines,

a plurality of gate lines,

a bias plane carrying a bias voltage,

a plurality of clamp lines electrically interconnecting the second TFT of each pixel of individual ones of the rows or columns of the array, wherein the clamp lines carry a clamping voltage,

a plurality of drain lines electrically interconnecting the plurality of data lines, wherein the drain lines carry a drain voltage, and

a sensor layer.

10. The full fill factor image array of claim 9, wherein the second TFT in each pixel is connected between the drain line and a storage node of the photodiode.

11. The full fill factor image array of claim 9, wherein the sensor layer comprises:

a collection electrode comprising a metal and N+ doped a-Si,

a continuous layer of undoped a-Si, and

a continuous layer of P+ doped layer of a-Si.

12. The full fill factor image array of claim 9, wherein the drain voltage is higher than the clamping voltage.

13. The full fill factor image array of claim 9, wherein the clamping voltage is higher than the bias voltage.

14. The full fill factor image array of claim 9, wherein the first TFT has an off voltage between about -5 to +25 V, wherein the off voltage is lower than the bias voltage, and an on voltage to transfer a charge from the photodiode to the data lines in less than about 10 microseconds.

15. A clamping circuit in a full fill factor sensor array that reduces lag and blooming comprising:

a gate line;

a data line;

a bias plane carrying a bias voltage;

a clamp line carrying a clamping voltage;

a drain line carrying a drain voltage;

a switching TFT having a source, a drain, and a gate, wherein the source or drain of the switching TFT is connected to the data line and the gate is connected to the gate line;

a photodiode having an anode, a cathode, and a storage node, wherein the anode is connected to the other of the source or drain of the switching TFT and the cathode is connected to the bias plane; and

a clamp TFT having a source, a drain, and a gate, wherein the gate of the clamp TFT is connected to the clamp line, the source or drain of the clamp diode is connected to the storage node of the photodiode, and the other of the source or drain of the clamp TFT is connected to the drain line.

16. A method for testing an array of TFTs during fabrication of a full fill factor sensor array comprising the steps of:

providing a plurality of pixel circuits, wherein each pixel circuit includes a clamping TFT and a switching TFT having a threshold voltage;

providing a plurality of data lines having a potential supplied by a charge amplifier

setting a clamp voltage to a DC gate voltage greater than the threshold of the switching TFT;

setting a drain voltage close to the potential of a data line; and

measuring a current flowing through the clamp TFTs and the switching TFTs each time the switching TFTs are on.

17. The method of claim 16, wherein the clamping TFTs' ability to turn off is tested by:

setting the clamp voltage to its off condition; and

measuring to verify a lack of current flow through the clamping TFT.

18. A method of globally resetting a sensor array comprising the steps:

providing a plurality of pixel circuits disposed in rows and columns, wherein each pixel circuit includes:

- a photodiode have a storage node to store a pixel charge

- a clamping TFT, wherein the clamping TFTs of individual rows or columns are electrically interconnected by clamp lines carrying a clamping voltage, and

- a switching TFT, wherein the switching TFTs of individual other rows or columns are electrically interconnected by drain lines;

pulsing the clamping voltage at a value to cause the pixel charge to be dumped to the drain lines.